

Amendments to the Claims

The listing of claims will replace all prior version, and listings, of claims in the application.

Listing of Claims**Claim 1 (Currently Amendment)**

A method for forming a junction region of a semiconductor device, said method comprising:

- providing a semiconductor substrate;
- forming a gate structure on said semiconductor substrate;
- implanting a dopant into said semiconductor substrate to form a junction region;
- forming an insulator layer on said gate structure and said semiconductor substrate;
- performing a carbon-containing plasma treatment [[for]] on said insulator layer, and said carbon-containing plasma is performed to penetrate the carbon atoms into said junction region;
- forming a spacer on a side-wall of said gate structure;
- implanting said dopant to form a source/drain region next to said junction region; and
- performing a heat treatment [[for]] on said semiconductor substrate.

Claim 2 (Cancelled)**Claim 3 (Currently Amended)**

The method of claim [[2]] 1, wherein the step of forming said spacer comprises:
conformally forming a nitride layer on said insulator layer; and
removing a portion of said nitride layer and said insulator layer to form said spacer.

Claim 4 (original)

The method of claim 1, wherein said junction region has a thickness of about less than 400 angstroms.

Claim 5 (original)

The method of claim 1, wherein said carbon-containing plasma comprises using a source containing carbon dioxide gas.

Claim 6 (original)

The method of claim 1, wherein said carbon-containing plasma utilizes a power on the order of 0.1 to 0.5 w/cm².

Claim 7 (Cancelled)

Claim 8 (original)

The method of claim 1, wherein said dopant is at least selected from the group consisting of one group III and group V element.

Claim 9 (currently amended)

The method of claim 1, wherein ~~said carbon-containing plasma is performed to penetrate carbon atoms into said junction region, and~~ the concentration of said carbon atoms in said junction region is around above 1e19/cm³.

Claim 10 (original)

The method of claim 1, wherein the temperature of said heat treatment for said semiconductor substrate is about 500 to 1200°C.

Claim 11(original)

The method of claim 1, wherein said heat treatment is selected from the group consisting of a furnace annealing treatment and a rapid thermal annealing treatment.

Claim 12 (Currently Amended)

A treatment method for forming junctions of a semiconductor device, said method comprising:

providing a silicon substrate;
forming a gate structure on said silicon substrate;
forming a first spacer on a side-wall of said gate structure;
implanting a dopant of boron into a portion of said silicon substrate to form a first doped region;
forming an oxide liner on said first spacer, said gate structure and said silicon substrate;
performing a carbon-containing plasma treatment ~~[[for]]~~ on said oxide liner;
forming a second spacer on said first spacer;
implanting a dopant of p-type into said portion of said silicon substrate to form a second doped region next to said first doped region;
performing a rapid thermal annealing treatment for said silicon substrate; and
forming a silicide layer on said gate structure and said silicon substrate.

Claim 13(original)

The method of claim 12, wherein said first doped region has a thickness of about less than 400 angstroms.

Claim 14 (original)

The method of claim 12, wherein said carbon-containing plasma comprises using a source containing carbon dioxide gas.

Claim 15 (original)

The method of claim 12, wherein said carbon-containing plasma utilizes a power on the order of 0.1 to 0.5 w/cm².

Claim 16 (original)

The method of claim 12, wherein said carbon-containing plasma is performed to penetrate carbon atoms into said first doped region, and the concentration of said carbon atoms in said first doped region is around above 1e19/cm³.

Claim 17 (original)

The method of claim 12, wherein said oxide liner is SiO₂.

Claim 18 (original)

The method of claim 12, wherein said second spacer is Si₃N₄.

Claim 19(original)

The method of claim 12, wherein the temperature of said rapid thermal annealing treatment for said silicon substrate is about 900 to 1200°C.

Claim 20(original)

The method of claim 12, wherein said silicide is self-aligned Co-silicide, such as CoSi₂.

Claim 21 (New)

A method for forming a junction region of a semiconductor device, said method comprising:

- providing a semiconductor substrate;
- forming a gate structure on said semiconductor substrate;
- implanting a dopant of group III or group V elements into said semiconductor substrate to form a junction region;
- forming an oxide liner on said gate structure and said semiconductor substrate;
- performing a carbon-containing plasma treatment on said oxide liner, and said carbon-containing plasma is performed to penetrate carbon atoms into said junction region;
- conformally forming a dielectric layer on said oxide liner;
- removing a portion of said dielectric layer and said oxide liner to form a spacer on said side-wall of said gate structure ;
- implanting a dopant of p-type ion into said semiconductor substrate to form a source/drain region next to said junction region;
- performing a heat treatment on said semiconductor substrate; and

forming a silicide layer on said gate structure and on the surface of said semiconductor substrate.

Claim 22 (New)

The method of claim 21, wherein said junction region has a thickness of about less than 400 angstroms.

Claim 23 (New)

The method of claim 21, wherein said carbon-containing plasma comprises using a source containing carbon dioxide gas.

Claim 24 (New)

The method of claim 21, wherein said carbon-containing plasma utilizes a power on the order of 0.1 to 0.5 w/cm².

Claim 25 (New)

The method of claim 21, wherein the concentration of said carbon atoms in said junction region is around above 1e19/cm³.

Claim 26 (New)

The method of claim 21, wherein the temperature of said heat treatment for said semiconductor substrate is about 500 to 1200°C.

Claim 27 (New)

The method of claim 21, wherein said heat treatment is selected from the group consisting of a furnace annealing treatment and a rapid thermal annealing treatment.